We claim:

1. A method for forming a metal interconnect in an integrated circuit device, the method comprising the steps of:
(a) depositing a metal seed layer onto a partially fabricated integrated circuit device;
(b) depositing a photoresist layer onto the metal seed layer;
(c) forming an opening in the photoresist layer by a photolithography process, thereby exposing a portion of the metal seed layer;
(d) depositing metal in the opening by a plating process;
(e) removing the photoresist layer and metal seed layer, thereby exposing the partially fabricated integrated circuit device;
(f) depositing a conformal barrier layer onto the metal; and
(g) depositing a dielectric material onto the partially fabricated integrated circuit device.

2. The method of Claim 1, wherein the metal seed layer is formed of a material to which the metal is directly plated.

3. The method of Claim 1, wherein the metal seed layer is copper.

4. The method of Claim 1, wherein the metal is deposited by an electrolytic plating process.

5. The method of Claim 1, wherein the metal is deposited by an electroless plating process.

6. The method of Claim 1, wherein the metal is copper, and the copper is deposited by an electrolytic plating process comprising the steps of:

immersing the partially fabricated integrated circuit device into a plating bath comprising a dissolved cupric salt; and

applying electric current to the metal seed layer.

7. The method of Claim 1, wherein the barrier layer is selectively deposited onto the metal by an electroless plating process.

8. The method of Claim 7, wherein the electroless plating process comprises the steps of:

depositing catalytic particles onto the surface of the metal; and

immersing the partially fabricated integrated circuit device into a plating bath.

9. The method of Claim 8, wherein the metal is copper; the catalytic particles are selected from a group consisting of palladium, cobalt and nickel; and the plating bath comprises a hypophosphite reducing agent.

10. The method of Claim 1, wherein the barrier layer is selected from a group consisting of CoWP, CoP, NiP, NiWP, CoB, NiB and CoWB.

11. The method of Claim 1, wherein the barrier layer is formed of an insulator material.

12. The method of Claim 1, wherein the barrier layer is deposited by a chemical vapor deposition process or physical vapor deposition process.

13. The method of Claim 1, wherein the barrier layer comprises a first layer of material selected from the group consisting of CoWP, CoP, NiP, NiWP, CoB, NiB and CoWB, and a second layer of insulator material.

14. The method of Claim 1, wherein the dielectric material is deposited by a chemical vapor deposition process, a physical vapor deposition process, or a spin-coating process.

15. The method of Claim 1, wherein the dielectric material has a dielectric constant of less than about 3.0.

16. The method of Claim 1, wherein the dielectric material comprises an organic polymer material, and is deposited by spin-coating the dielectric material onto the partially fabricated integrated circuit device.

17. The method of Claim 1, wherein the dielectric material comprises a carbon-doped silicate glass, and is deposited by a plasma-enhanced chemical vapor deposition process.

18. The method of Claim 1, further comprising the step of:
(h) removing excess dielectric material and the top portion of the barrier layer, thereby exposing the top surface of the metal.

19. The method of Claim 1, further comprising repeating steps (c) through (e), prior to performing step (f).

20. The method of Claim 1, further comprising, prior to step (a), the step of:
depositing a conductive barrier liner onto the partially fabricated integrated circuit device.